Physical Design Methodology Best Practices
NANOMETER AND RTL-DOWN CLOSURE

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IEEE DATC Electronic Design Processes Workshop
Monterey, CA

April 9-10, 2001
SOC design opportunities & challenges

- **First-to-Market & Volume SOCs → Business Success**
  - No market ... for a 2nd to market
  - 3-months late = $500M loss

- **Limited design capacity**
  - Competitive new products roadmap
  - Customize products
  - Access new processes first
  - Multiple sourcing

- **Rapid increase in design complexity**
VLSI → SOC: Rapid increase in design complexity

- 0.5um → 0.18um
- 5x5 mm² → 21.7x21.3 mm²
- ~0.8 → 287.5M transistors
- 3LM → 6LM
- ~50 → 150 MHz (#>500MHz)

#: Cirrus Logic, Inc. IC, 3Ci™
VLSI → SOC: Hierarchical design approach

- SOC Design = IP block creation + block integration

- Enable concurrent engineering
- Reduce development complexity
- Simplify program management
- Leverage proven IP blocks
  - Improve TTM, TTV and quality
  - Reduce technical, schedule risks
- Leverage platform infrastructure
  - Verification, Validation
Top-level SOC design methodology

- **Functional design** → hierarchical
- **Electrical / physical design** → hierarchical
- **IP leverage; Customer-specific design**
Block-level design methodology

- Architectural optimization (timing)
- Inter-group buses, bandwidth
- Clock, SI, test; validation

- Custom WLM (or better)
- Power, clock, test reqmts. added
- Critical blocks (e.g., ECC)

- Top-, block-specific CWLM-based (or better)
- With added constraints

- Top, block clock design
- I/O driver, padring design
- Noise minimization, isolation
- Power distribution (Internal, I/O)
- Board-level timing, SI

- Scan stitching, re-ordering

- Full RC back-annotation
- Hierarchical “black-box” models
Sony Computer Entertainment: GS® I-32

- Enhanced architecture: 8x higher eDRAM vs. PS®2 GS®

- Performance
  - eDRAM Bandwidth = 48 GB/s
  - Buses >2K bits wide
  - Render 75M polygons/s

- SOC integration
  - 280M + 7.5M transistors
  - 21.7 x 21.3 mm²

- Scale
  - >400K components
    - 11 blocks, 31K-218K gates
    - >68K flip-flops
  - >500K signal nets
    - >2K nets >10 mm. long

- 0.18 um, 6-metal CMOS
Design approach

- Fully-hierarchical design: Netlist to tape-out in 10 weeks

Design challenges
- Power distribution
- Clock architecture
- Timing design
  - Load modeling
  - Delay calculation
- Signal Integrity
  - Buffer insertion
  - Crosstalk
Accurate fully-hierarchical delay calculation

- Fully-hierarchical block-based timing analysis
  - Analyze large designs (scalable capacity)
  - Enable concurrent design
  - Faster timing convergence, verification (STA)

- Signal paths traverse hierarchy
  - Block inputs with ~0 – 2 mm. metal → RC delay

- Model block boundary pin input RC as $C_L$
- $C_L$ → timing inaccuracies when RC significant
Accurate fully-hierarchical timing

- \( C_L \) over-estimates RC delay
  - Latent hold time defects
  - Setup \( \rightarrow \) overdriven
- ECSM \( (C_{eff(50\%)} ) \) fits SPICE at threshold
- ECSM \( \rightarrow \) \( \approx 2\% \) correlation to SPICE for complex topologies

**Diagram Description**

- Voltage (V) vs. Time (ns) graph
- \( C_{eff(50\%)} \)
- \( C_L \)
- \( B1 \)
- \( B1' \)
- \( IC \)
- \( +2\% \) correlation between ECSM and SPICE

**Graph Details**

- Voltage range: 0 to 15 V
- Time range: 0 to 1.6 ns
- Delay range: 1.43 to 1.56 ns
**Signal integrity**

- **Insert buffers ~1.5 - 2.5 mm.**
  - Bound timing uncertainty
  - Reduce total delay

- **Address impact in Static Timing Analysis**
  - Reduce setup time margin
  - Bounded hold time margin
IC design → design methodology, technology

- Hierarchical (mixed-signal) design
  - Fully-hierarchical timing: Enhance concurrent design

- Power distribution

- Clocking architecture

- New design technology
  - Nonlinear delay calculation technology
  - Black-box, gray-box modeling
  - Signal integrity
    - RC transmission line effects
    - Crosstalk management
    - Buffer insertion

- 0.15um – 0.13um work
  - Technology validation, signal integrity, RLC, substrate, others

- Focus on silicon engineering: First silicon success
Related reading

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