Reliability Challenges in Advanced Packaging

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More Than Moore is how packaging will play a crucial role in maintaining Moore’s Law.

However, reliability does not always have a seat at the table.
Major Challenges in Reliability of Advanced Packaging

**Key Mechanisms**

- Low-K Cracking
- Solder Joint Fatigue
- Microvia Separation

**Key Drivers**

- New Materials
- 2.5D/3D Packaging
- Extended Lifetimes
LOW-K CRACKING
WHAT IS ELK / ILD CRACKING?

• Metal layers (Cu) send power and route signals from the active region (transistors)
• Each metal layer has an inner layer dielectric (ILD) composed of some form of SiO\(_2\)
• Elevated mechanical/thermo-mechanical stress will crack the ILD
ELK/ILD CRACKING (cont.)

• Known issue for over 15 years
  - Described as ‘white bump’ based on acoustic signature

• Has typically occurred at either flip chip attach or underfill cure processes

• One of the big drivers for switch to low Tg (underfill)

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Thursday, July 3rd 2008
NVIDIA Admits to Selling Faulty Mobile GPUs, Shares Plummet
NVIDIA Admits to Selling Faulty Mobile GPUs, Could Cost it up to $200 M
Why is ELK Cracking Becoming More Prevalent?

- Combination of transition to ELK/ULK dielectric material and transition to copper pillar and larger die

- Lower k (ELK/ULK) material is weaker and softer
  - By comparison, glass has a $G_{lc}$ of 7 J/m$^2$

- Copper has a much higher (2X) modulus than solder
  - Drives a lot more stress into the ILD

WHY IS ELK CRACKING BECOMING MORE PREVALENT?

• Increasingly, failures are detected/occurring during thermal cycling
  - Not flip chip attach and not underfill cure

• Key issues
  - The interplay between applied and residual stresses
  - Debate about the presence or absence of cracks
  - Possibility of things changing over time
  - Poor/insufficient approaches to mitigation

R. Katkar et. al., Reliability of Cu Pillar on Substrate, 2011
APPLIED VS. RESIDUAL STRESS

• Difference in coefficient of thermal expansion (CTE) between die and substrate causes a moment on the copper pillar
  - Drivers compressive and tensile normal stresses in ELK layer

• Therefore, the corner I/O is typically the bump of concern
APPLIED VS. RESIDUAL STRESS (cont.)

• The interplay between applied stresses and residual stresses are not necessarily well understood

• Higher temperatures during thermal cycling increase applied stresses, but lowers residual stresses

• Real risk that standard JEDEC thermal cycling can not be extrapolated to field conditions
  - -40°C to 10°C > -40°C to 125°C?
  - Where have we seen this before?
CRACKS OR NO CRACKS?

• Modeling and mitigation approaches change if ELK cracking is driven by the presence of an initial crack (i.e., during die singulation)
• The presence of an initial crack may explain time-dependency of ELK cracking

Fig. 2. Submodel of the BEOl stack in a FC-assembly

Fig. 3. Normalized ERR at the crack tip with and without an initial crack in the global model

Energy Release Rate (ERR)

ELK CRACKING OVER TIME

• Failure after several hundred cycles does not correlate with typical brittle fracture
  - Brittle fracture is typically deterministic (binary)
  - It either fails or it doesn’t

• Theory 1: A material property is changing over time
  - Work hardening of solder? Degradation increases compliance
  - Work hardening of copper? Requires high stresses (100 to 200 MPa)
  - Work hardening of polyimide? Not reported in the literature
ELK CRACKING OVER TIME (cont.)

- **Theory 2**: Microdamage Evolution / Brittle Fatigue
- Softer material with intentional stress concentrations (porosity) could drive fatigue crack growth
  - Growth until it reaches a critical size

POOR/INSUFFICIENT APPROACHES TO MITIGATION

• Mitigation is dominated by design rules
  - Limited to no correlation to actual stress states within the ILD

• Examples of design rules
  - Large pad diameter
  - Rigid requirements regarding metal density
  - Coarser spacings
  - Copper pillar dimensions

• Different design rules from different suppliers (foundry vs. OSAT)
TRANSITIONS ARE KEY

• Strong indication that design guidelines on metal density are insufficient

Fundamental and Applied Fracture Characterization of Thin Film Systems
TRANSITIONS ARE KEY (cont.)

• Transition between different dielectric materials
  - ULK/ELK to LK, ULK/ELK to USG, etc.

• Large variation in areas of metal and dielectric under bond pad

• Large variation in concentration of vias under or adjacent to the bond pad

SOLDER FATIGUE
SOLDER JOINTS FATIGUE UNDER THERMAL CYCLING

Solder is connecting two objects that expand/contract at different rates
Knowing the critical drivers for solder joint fatigue, we can develop predictive models and design rules.
1D STRAIN ENERGY

$$\Delta \gamma = C \frac{L_d}{h_s} \Delta \alpha \Delta T \quad (\alpha_2 - \alpha_1) \cdot \Delta T \cdot L = F \left( \frac{L}{E_1 A_1} + \frac{L}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left( \frac{2 - \nu}{9 \cdot G_b a} \right) \right)$$

$$\Delta W = 0.5 \cdot \Delta \gamma \cdot \frac{F}{A_s} \quad N_f = \left( 0.001 \cdot \Delta W \right)^{-1}$$

Closed Form, PCB Stiffness, Strain Energy, E (T), Tg, Die Shadow

3D STRAIN ENERGY

\[ N_0 = K_1(\Delta W_{avg})^{K_2} \]
\[ \frac{da}{dN} = K_3(\Delta W_{avg})^{K_4} \]
\[ N_f = N_0 + \frac{D}{da/dN} \]

GLOBAL + LOCAL MODELING
UNEXPECTED SOLDER FAILURES

Increasing number of companies reporting early life failures during thermal cycle testing or in the field

Classic solder fatigue approaches do not seem to be capturing these risks
Strong indication that mixed-mode stresses are key drivers

CLASSIC BEHAVIOR

- Idealized CTE mismatch

\[ \gamma = \frac{CL_h \Delta T \Delta \alpha}{h} \]

High Temperature

T = 20°C

Die CTE = 2.6 ppm/°C

Substrate CTE = 14 ppm/°C

T = 120°C
Strong indication that mixed-mode stresses are key drivers

MIXED-MODE (TRIAXIALITY) BEHAVIOR
• Driven by increasing complexity and density of electronics, including adoption of mechatronics

• Three categories
  - Over-Constrained Boards / Housing Interaction (previously covered)
  - Potting/Coating/Underfill
  - Mirroring

• Also described as ‘system-level’ effects
OVER-CONSTRAINED BOARDS
COATING/POTTING/UNDERFILL

\[ E = \frac{\Delta T (a_2 - a_1)}{A E_1 + 1} \]

- Solid: E
- Dashed: CTE

Temperature (°C)

Temperature Change (°C)

Tensile Stress (MPa)
Avoided in earlier designs (challenges with rework and X-ray inspection)
- Increasingly required due to higher densities and higher speed memory

Reduces lifetime by 1.5X to 5X, but numerous organizations struggle to predict behavior

Based on Darveaux Model

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SYSTEM-LEVEL SOLDER FATIGUE PREDICTION

• Sherlock (Thermo-mech)

• Creep equivalent approach (Secant Modulus)
  - No time-stepping

• Energy partitioning method of shear and axial components
  - Energy calculated using closed-form equation

\[ N_f = C_1(\Delta W)_{shear}^{n_1} + C_2(\Delta W)_{Axial}^{n_2} \]
SIMULATION AND RELIABILITY OF ADVANCED PACKAGING
LOW-K CRACKING AND SOLDER FATIGUE MITIGATION

• Increasingly, failures are occurring ‘randomly’ throughout the advanced package
  - No longer only occurring at the corners (1\textsuperscript{st} level or 2\textsuperscript{nd} level interconnect)

• Even for packages that are ‘similar’ and follow all design rules

• Driven by increasingly package complexity (different materials, different stress states)
  - Low K cracking: metal layout, bump layout and bump collapse
  - Solder fatigue: array pattern, system effects, microvia stacks
MODELING CHALLENGES – SOLDER FATIGUE/MICROVIA STACKS

- Where and what of microvia stacks increasingly driving solder fatigue and low-k cracking behavior
- How to perform global/local without knowledge of what to model and where to model?
NEXT STAGE IN MODELING/SIMULATION OF ADVANCED PACKAGING

• ANSYS is extending scripting, modeling and element options to expand the ability to model all artifacts that could influence key failure modes
  - Interconnect geometries + die, interposer, substrate and PCB layout

• Combined with expansion of electronic material properties