Validation Strategies with pre-silicon platforms

Shantanu Ganguly

Synopsys Inc
April 10 2014
Agenda

- Market Trends
- Emulation HW Considerations
- Emulation Scenarios
- Debug
Mobile & Internet-of-Things Driving Growth

Convergence → SoC complexity → New verification challenges

Verification Complexity
Power Efficiency
More Software
Time-to-Market
SoC Multi Core Architecture Trends

- Massive feature integration
  - Driven largely by Moore’s Law (supply) and convergence (demand)
- Distributed architectures
  - Higher scalability (and independence)
  - Sharing memory
- Multiple processors
  - (Multicore) CPU
  - DSP
  - Special purpose (MPEG, GFX, …)
  - Always on controller
- Distributed DMA
  - Removes centralized DMA bottleneck
- Increasing software complexity
  - Re-use with multiple platform SoCs
  - Broader end use market coverage per SoC with software programmability

From NIT Alumni Meet Keynote Speech: Jim Hogan
SoC Design Complexity & Cost – Out of Control

- Increasing complexity means increased risk
  - At 32nm, a typical design has ~50% chance to meet all objectives
  - At 22nm, that number drops to ~30%

- “Designer productivity must improve to match chip complexity”
  - The later a problem is detected, the more impact it will have on design schedules

Source: I.B.S. Inc.

Source: Gartner
Need ‘Shift-Left’ for Faster Time-to-Market

Earlier HW verification, earlier SW bring-up

SoC Bugs Found per Week

Static & Formal
Automate Setup
VIP

Debug

Earlier…
Virtual Platforms
Fast Emulation
HW-SW Bring-up
Virtual & FPGA Prototyping

Project Time

Faster Simulation

Smart Verification Strategy
- Static and Formal

Intelligent Verification Methodology
- Integrated, automated flows

Earlier HW-SW Bring-up
- Faster emulation

Verification Continuum
- Seamless flow
Agenda

- Market Trends
- Emulation HW Considerations
- Emulation Scenarios
- Debug
Three Ways to Emulate 256 Million Gates

- Emulation chip capacity accounts for the wide range of sizes.

Custom Processors

Commercial FPGAs

Custom FPGAs

1 meter
### Custom Emulation Chip Advantages

|                          | **Custom FPGA**                                                                                                                                                                                                 | **Custom Processor**                                                                                                                                                                                                 | **Commercial FPGA**                                                                                                                                                                                                                                                                                                                                 |
|--------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| **Compile Time**         | Faster due to emulation-specific interconnect architecture.                                                                                                                                                       Faster due to processor-type architecture.                                                                                                                                                                                                                                          Slower due to chip place & route. Easily run on parallel on a small server farm.                                                                                                                                                                                                                                                                   |
| **Debug**                | Built-in: Change probes without recompile.                                                                                                                                                                         Built-in: Change probes without recompile.                                                                                                                                                                                                                                          Mix of built-in (readback) and FPGA resource. Some probe changes require recompile.                                                                                                                                                                                                                                                                     |
Commercial FPGA based solution superior for Emulation

• Highest capacity per chip
  – ZeBu Server 3 module emulates 60M gates in 9 emulation chips.
    – Palladium XP needs 54 chips, Veloce 2 needs 75 chips.
  – Components fit better, fewer design nets get cut.

• Means less interconnect HW
  – Highest performance: 2 to 5 MHz
  – Low power, small size, reliable

• Latest process every two years
  – From Xilinx, no development cost

== Lowest TCO
  – Fastest, coolest, smallest, cheapest, most reliable logic emulation.
ZeBu Server-3 Hardware Performance Advantage

- 6-8X larger capacity emulation chips
  - fewer nets must cross chip-to-chip,
  - more nets stay on-chip where they are fast

- High bandwidth communication between emulation chips, modules, units, host
  - Each chip has 600 Gbps bandwidth to other chips
  - 33 Gbps bandwidth between modules
  - 640 Gbps bandwidth between units
  - 4 Gbps host communication bandwidth

- FPGA architecture advantages
  - Specialized HW for arithmetic operations in FPGA.
  - Wire-to-wire and gate-to-gate mapping, no modeling abstraction

<table>
<thead>
<tr>
<th>Application</th>
<th>Design Size</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPU Quad Cluster</td>
<td>60 MG</td>
<td>5.0 MHz</td>
</tr>
<tr>
<td>GPU Dual Cluster</td>
<td>40 MG</td>
<td>4.95 MHz</td>
</tr>
<tr>
<td>GPU Single Cluster</td>
<td>33 MG</td>
<td>4.75 MHz</td>
</tr>
<tr>
<td>Customized GPU</td>
<td>50 MG</td>
<td>3.75 MHz</td>
</tr>
<tr>
<td>Communication</td>
<td>60 MG</td>
<td>2.9 MHz</td>
</tr>
<tr>
<td>Processor</td>
<td>60 MG</td>
<td>2.9 MHz</td>
</tr>
<tr>
<td>Consumer SoC</td>
<td>100 MG</td>
<td>2.8 MHz</td>
</tr>
<tr>
<td>Broadband SOC</td>
<td>80 MG</td>
<td>2.5 MHz</td>
</tr>
</tbody>
</table>
ZeBu Server-3 Throughput Advantage

- Highest raw performance hardware
- Multi-threaded runtime
- Truly concurrent communication message port
  - No blocking message transfer
- Dedicated high speed HW resources for implementation of transactors and communication ports.
- Each transactor can be modeled as separate process for maximum parallelism.
Agenda

• Market Trends
• Emulation HW Considerations
• Emulation Scenarios
• Debug
Verification: Architecture to Silicon

Accuracy

Architecture Exploration

Does the architecture meet performance and power requirements?

Processor & GPU selection
Memory System Dimensioning
Interconnect Configuration
Cache Coherency
Global Interrupts
Power Management

Design Technology:
Traffic Models
Transaction Level Models
Performance Visualisation
Hybrid-Simulation

HW / SW Integration

Prototype SW before first silicon

OS Integration
Driver Development
Virtualisation
Performance Optimisation

Tools:
Debugger
Transaction Level Models
systemC Virtual Prototypes
FPGA Prototypes
Performance Visualisation

Functional Verification

Does the design function correctly & meet performance and power requirements?

Protocol Compliance
Interconnect BW & Latency
Cache Coherency
Data integrity
Power & Clock Domains

Design Technology:
Traffic Models
Verification IP
System Monitor
Performance Visualisation

System Validation

Validate that the design functions as specified.

Graphics
Video
Audio
Browser Application
Gesture recognition
Phone functions
Camera functions

Design Technology:
FPGA Prototypes
HW Accelerated Simulation
Hybrid-Simulation
Verification IP
Transaction Level Models
IO Traffic

Turn Around Time
## Common HW-Assisted Verification Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Host Workstation</th>
<th>External Hardware</th>
<th>Target System</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Simulation</strong></td>
<td>Simulator</td>
<td>DUT</td>
<td></td>
</tr>
<tr>
<td><strong>In-Circuit Emulation (ICE)</strong></td>
<td></td>
<td>DUT</td>
<td>Buffer</td>
</tr>
<tr>
<td><strong>Embedded Testbench</strong></td>
<td>DUT</td>
<td>Emulator</td>
<td>Object Code</td>
</tr>
<tr>
<td><strong>Co-Simulation (Signal-Level)</strong></td>
<td></td>
<td>DUT</td>
<td>Emulator</td>
</tr>
<tr>
<td><strong>Transaction-Based Verification (TBV)</strong></td>
<td>Virtual Peripheral</td>
<td>SCEMI/ZEMI</td>
<td>DUT</td>
</tr>
</tbody>
</table>
# Summary of Verification Modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>External Hardware</th>
<th>Challenges</th>
</tr>
</thead>
</table>
| Simulation                    | • Everyone has one  
• Perfect for 90% of designs                                                     | • Never fast enough                             |
| In-Circuit Emulation (ICE)    | • Highest performance  
• Physical connections                                                              | • Rate adapter availability                     |
| Embedded Testbench            | • Very fast  
• No physical connections                                                           | • Needs synthesizable TB  
• Limited to Software only                                                            |
| Co-Simulation (Signal-Level)  | • Simple to use  
• Leverages existing TB  
• Good for DUT bring-up                                                               | • Little performance gain                       |
| Transaction-Based Verification (TBV) | • Highest performance  
• Works with virtual devices  
• No rate adapters needed                                                             | • Availability of transactors                   |
One Emulator, Many Applications

Advanced verification use modes with ZeBu Server-3

- **Transaction-based Verification**
  - system-level SoC verification

- **Hybrid Emulation**
  - architecture optimization & early software development

- **Simulation Acceleration**
  - up to 100x simulation performance

- **In-circuit Emulation**
  - real-world connections

- **Power-aware Emulation**
  - UPF support and SAIF output

- **Synthesizable Testbench**
  - higher performance
Environment for In-Circuit Emulation

Physical Test Environment

Emulator

- DDR Memory Interface
- Flash Memory Interface
- NTSC TV Interface
- LCD Display Interface
- Terminal Interface
- Digital Still Camera Interface
- Keypad Interface
- USB 2.0 Interface
- Ethernet 10/100 Interface
- I2S Audio Interface
- JTAG Interface

SoC Prototype

- ARM11 Core
- DSP Core
- Logic
- Memory

© 2014 Synopsys. All rights reserved.
Transaction-based Verification Environment
ZeBu Power Analysis Generates Power Profiles

- Ideal for block and system-level analysis with hardware and software
- Captures every transition within each clock period
  - User-programmable: blocks, registers, buses, entire SoC
- Includes cumulative total spanning user-defined clock numbers
  - Large span for highest performance
  - Short span for highest accuracy
- Works seamlessly with PrimeTime

Unexpected power spike

Focus to identify source

SAIF or FSDB files
ZeBu Hybrid Emulation

Architecture optimization and early software development

- RTL runs at high speed in ZeBu while processor model or other components run in virtual prototype
- Reduces need to have high level models for all components
Agenda

• Market Trends
• Emulation HW Considerations
• Emulation Scenarios
• Debug
Why Is SoC Debug so Complex?

- Constraints
- Coverage
- Software
- TestBench
- UPF
- Embedded Processor
- Analog
- Bus Protocols
- VIP
- RTL/Gate
- Analog
**Verdi³’s Unique Technology**

- **Debug Oriented DB**: Optimized for debug
- **De facto Standard FSDB**: De facto Standard FSDB
- **Simulator Verification and Platform Independent**: Siloti

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock Tree Extraction/Debug</td>
<td>Trace This Value</td>
</tr>
<tr>
<td>Power-Aware Debug</td>
<td>Trace Active X</td>
</tr>
<tr>
<td>Simulator Verification and Platform Independent</td>
<td>Assertion Analysis</td>
</tr>
</tbody>
</table>

- Database is not optimized for debug

**Debug Automation**

- **Native Debug A**
- **Native Debug B**
ZeBu Simulator-Like Debug with Verdi³

- **Full visibility (RTL & gate level)**
  - All registers, nodes, memories
  - Run-time and post-run debug
  - No recompiles required
- **Open standard support**
  - FSDB, VCD, etc.
- **Transaction level debug**
- **iCSA integration for fast time to waveform**

**RTL & Gate-Level Hierarchical Debug**

**Runtime Control**

**Verdi³ Waveform**
Complex Debug Scenarios

- **Cache Coherency Error**
- **Boot OS** (Bootloader, Kernel, Init, VM, etc.) (1 billion clocks)
- **System Services** (Pwr, Batt, NetStat, Bluetooth, etc.) (1 billion clocks)
- **User Applications** (Internet Browser)

**Problem:** Symptom happens far later than bug… Root cause cannot be traced.

2+ billion clocks

- **Reset** (1000 clocks)
- **Boot OS** (1 billion clocks)
- **System Services** (1 billion clocks)
- **User Applications**

Typical Logic Analyzer Trace Depth (1 million samples)
ZeBu Post Run Debug

Billion-Cycle Full Visibility, Optimized for HW/SW Co-Verification

- Testbench captures DUT state periodically
- DUT inputs captured on every clock
- Data stored on Host PC disk drive
- To debug, user selects a restore point… and loads it into ZeBu to generate waveforms

Host Machine

- User Applications (Internet Browser)
  - Data stored on Host PC disk drive
  - To debug, user selects a restore point… and loads it into ZeBu to generate waveforms

System Services (Pwr, Batt, NetStat, Bluetooth, etc.)
- (1 billion clocks)

Boot OS (Bootloader, Kernel, Init, VM, etc.)
- (1 billion clocks)

Reset
- (1000 clocks)

CPU Clocks

© 2014 Synopsys. All rights reserved.
HW/SW Debug Overview

*Embedded Processor Debug with Synchronized RTL, C, Assembly*

- Enables co-debug between RTL and SW
- HW and SW debug synchronized in time
- View C/Assembly source, C variables, stack, memory
- Debugs multiple core simultaneously
- Supports all popular cores
- Easy to support additional cores or custom cores
- Custom Core support without exposing CPU internals

![Diagram](image)
HW/SW Debug Use Models

Verification Environment with C-Tests

- Part of SoC verification schedule
- Hardware debug with C-tests/stimulus
- C-tests may have minimal OS or boot code
- Requires concurrent software and hardware debug

Use HW/SW Debug for this task

Driver Development

- Software (driver) development
- Fast speed is required (>1MHz)
- Approximate hardware is acceptable

Use Virtualizer for this task

Prepare for First Silicon Bring-Up

- Debug synthetic tests mimic specific use scenarios
- Tests run on a bare-metal OS
- Develop and bug tests on a pre-silicon model
- Get ready for silicon bring up

Use HW/SW Debug for this task

First Silicon Debug

- Observed failure running test on first silicon
- Debug the failure and isolate a design bug
- Create/Validate software/firmware workaround

Use HW/SW Debug for this task
The End