FPGA Entering the Era of the All Programmable SoC

Ivo Bolsens, Senior Vice President & CTO
Moore’s Law: The Technology Pipeline

Logic Device Roadmap

- **V_{dd}**: 1.0/1.1V, 0.9/1.0V, 0.8/0.9V, 0.7/0.8V, 0.6/0.7V, 0.5/0.6V, < 0.5V

- **Advanced Gate Stack Engineering**
- **Fully-depleted Channel Electrostatics**
- **Band-Engineered Channel for Enhanced Transport**
- **New Transport & Extreme Channel Electrostatics**

- **Metal Gate + High-k**
- **Multigate FETs / FDSOI**
- **III/V & Ge channels**
- **Nanowires Tunnel FETs**

- **Novel Materials**
  - 2D Quantum Materials, (graphene, topological insulators) spintronics

- **Tech Node**
  - 32/28nm
  - 14nm
  - 7nm
  - 5nm

- **imec**

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The last 50 years of the semiconductor industry have been all about the manifestation of Moore's Law with regard to the dimensional scaling of Integrated Circuits (ICs). As consumers of electronic devices, we all love to see better products at a lower cost with each and every new product cycle. But now storm clouds are forming.
Design Cost


- **Design cost ($M)**
- **Mask cost ($M)**
- **Embedded software ($M)**
- **Yield ramp-up cost ($M)**

28/22-nm

32-nm

45-nm

65-nm

90-nm

130-nm

180-nm

28nm = 2x 45nm cost

> $170 M

($ Million)
What Happens in an Internet Minute?

- 639,800 GB of global IP data transferred
- 135 Botnet infections
- 1,200 New mobile users
- 20 New victims of identity theft
- 204 million Emails sent
- 47,000 App downloads
- 83,000 In sales
- 61,141 Hours of music
- 20 million Photo views
- 320+ New Twitter accounts
- 100,000 New tweets
- 277,000 Logins
- 6 million Facebook views
- 2+ million Search queries
- 30 Hours of video uploaded
- 1.3 million Video views
- Today, the number of networked devices = 1
- By 2015, the number of networked devices = 2x
- In 2015, it would take you 5 years
- To view all video crossing IP networks each second

And Future Growth is Staggering
“Don’t believe everything you read on the Internet.”

Abraham Lincoln, U.S. President
The energy market is undergoing a major transformation…

Smart Factories
For factory management in the future, it will become essential to strive to implement smart capabilities…

Smart wireless networks to the rescue
Carriers are turning toward more intelligent network management…

From Dumb Pipes to Smart Networks
Trend Wired Infrastructure: Software Defined Networks

Trend Wireless Infrastructure: Scalable Platforms

**Capacity**

**Indoor**
- **Residential Femto**: 4-16 Users, <100mW
- **Enterprise Femto**: 30-60 Users, <250mW
- **Office**: 30-200 Users, <1W
- **Dense Indoor** (Malls, Transport Hubs): 30-200 Users, <1-10W

**Outdoor**
- **Macrocell + Active Antennas**
- **Macrocell**
- **Microcell**
- **Wide Area**
  - 2-3x Data Capacity of RRU
  - ~200 Users/sector
  - 20-100W Multi-Sector

**Coverage**
- **Home**
- **Office**
- **Dense Indoor** (Malls, Transport Hubs)
- **Urban Infill**: ~200 Users, <1-10W Single Sector

**Wide Area**
- ~200 Users, 20-100W Multi-Sector
Trend Data Center Infrastructure: Cloud Computing

Big Data
Increasing Volume, Velocity, and Variety

Low power
Reduce operation and cooling costs

Security
Both outside and inside
Industry Mandates

Programmable Imperative

Programmable Systems Integration

Insatiable Intelligent Bandwidth
The Era of All Programmable SoC
CPU + FPGA Evolution

2005

FSB

PCle

Up to 4.2GB/s Platform Bandwidth

2011

PCIe

PCIe

FSB/QPI

Equal BW: FSB vs PCIe

PCIe IO Device

Cache Flush

Device Driver Call

FSB/QPI: 2x PCIe BW

In-Socket Accelerator

Direct Cache Access

Shared Memory Function

Bandwidth

GBit/s

2005 2006 2007 2008 2009 2010 2011
Extended Processing: Embedded ARM

- Processor System boots first
  - Separate power for PL*
  - Peripherals alive before PL configuration

- Processor controls PL configuration
  - Multiple security levels supported
  - Boot in secure or non-secure mode
  - Download PL image via network, SD, USB

- Multiple AXI interfaces to PL
  - Processor System can access IP in PL
  - PL IP has access to Processor System peripherals and memory system at full BW

*PL = Programmable Logic
Programmable Platform Opportunity

**Metric**

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>&gt; Double</th>
</tr>
</thead>
<tbody>
<tr>
<td>Latency</td>
<td>4x lower</td>
</tr>
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</table>

Major Leap in Cost and Performance
FPGA/CPU Use Models

0. Pipelined datapath
   - HDL programmed

1. Pipelined datapath with SW control
   - CPU sets register values

2. CPU + FPGA co-processing
   - FPGA part of explicit address space

3. CPU + FPGA peer processing
   - Cache Coherency
Programmable Platform: CPU + FPGA Peer Processing

Coherency Benefits:
- **Peer Processing**: Direct Cache-2-Cache data movement
- **Latency**: Very low latency access to CPU (FPGA) data
- **Usability**: No SW cache flush needed

Capabilities
- Coherent Caches for HW
- Coherent Caches for SW
- Coherency Management
Design Flow Overview

Software Design Flow

Software Development

Profiling

SW/HW Partitioning

Software Refinement

Vivado HLS Refinement

SW Compiler

HW Synthesis

Executable

Bit Stream
Programming Accelerators from C/C++

C/C++ Source → Serial application on standard processor → Dynamic library call → C Inner Loop

Compile directly from C to FPGA-ISA → ARM → High-performance interconnect → ZYNQ → Parallel algorithm On FPGA
Programming Accelerators from C/C++

- Enables software programmers to target Xilinx FPGAs
  - Software-programmability
  - Portability: 7 series, Zynq

- Delivers productivity increase for RTL designers
  - C/C++ level verification and testbench reuse
  - Earlier area/latency reports
  - Software-driven design exploration

More Turns Per Day (Verification and Architecture Exploration)
Quality of Results

FPGA: >38 times better performance than DSP video processor
QOR: C2FPGA equal to or better than RTL synthesis
Ease-of-use: C2FPGA 2x fewer lines of C code than DSP processor
Vivado IP Integrator
Enabling Reuse and Delivering Fully Functional IP Subsystems

IP Packager
- Source (C, RTL, IP)
- Simulation models
  - Documentation
  - Example Designs
  - Test bench

Standardized IP-XACT

- Uses multiple plug-and-play forms of IP to implement functional subsystem
- Includes software drivers and API
- Accelerates integration and productivity
Vivado IP Integrator
Intelligent IP Integration

» Co-Optimized for platforms
  – Target platform aware
  – Supports All Programmable Zynq and 7 series kits

» Co-Optimized for silicon
  – IP aware automated AXI Interconnects for maximum performance or area
  – Automated interface, device driver & address map generation for Zynq and MicroBlaze
Automated IP Subsystems
- Block automation for rapid design creation
- One click IP customization

Correct-by-construction
- Extensible IP repository
- Real-time DRCs and parameter propagation/resolution
Cost and power reduction by integrated solution

Performance increase by exploiting the massive compute power of multi-core processors and programmable logic
Programmable Digital Pre-Distortion

DPD negates PA non-linearity
- PAs consume massive static power
- DPD improves PA efficiency by ~35-40%

\[ y_0 = \text{PA}(z) = x \times \text{CC} + \text{AMC} + \text{Alignment} \]
HW Acceleration

70x speed-up for VW

Update Time (ms)

0 250 500 750 1000 1250

Original Optimized NEON PL Accelerator

Algorithm optimization A9 SW optimization Vivado HLS optimization

Cholesky VW Alignment

3% ZC7020

320ms
HW Accelerator Resources

- Unroll=1
  - DSP: 2305
  - FF: 2352
  - LUT: 16

- Unroll=2
  - DSP: 2882
  - FF: 3243
  - LUT: 28

- Unroll=4
  - DSP: 5200
  - FF: 4293
  - LUT: 52
DPD Architecture Data Movement

Reduced Resources Because of AXI4Lite Infrastructure
DPD Architecture Data Movement

High Throughput Because of DMA Infrastructure

AXI4 Interconnect

AXI4 Lite Interconnect

AMBA® Switches

General Interrupt Controller

512 KB L2 Cache

Timers / Counters

NEON™/FPU Engine

Cortex™-A9 MP Core™

32/32 KB I/D Caches

Snoop Control Unit (SCU)

256 KB On-Chip Memory

DMA

Configuration

Memory

AXI DMA

Accelerator

ARM® CoreSight™ Multi-core & Trace Debug

NEON™/FPU Engine

Cortex™-A9 MP Core™

32/32 KB I/D Caches

512 KB L2 Cache

Snoop Control Unit (SCU)

256 KB On-Chip Memory

DMA

Configuration

<table>
<thead>
<tr>
<th>FF</th>
<th>LUT</th>
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<tbody>
<tr>
<td>&gt;3000</td>
<td>&gt;3000</td>
</tr>
<tr>
<td>Accelerator</td>
<td>5200</td>
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High Throughput Because of DMA Infrastructure
Hardware/Software Boundary

Optimal cut point depends on execution times and cost of communication

Implement different cut points is a time consuming task

Goal: Maximize Throughput and Reduce Area Resources
Smart Software Driver is Necessary
HW/SW Design Flow

- CPU
  - C-compiler
  - SW-drivers
  - AXI
- FPGA
  - C-synthesis
  - Libraries
  - Wires

- Application
- Platform

- Concurrent SW
- Middleware
- Hardware

- Data Movement Interconnect
  - Video Codec
  - Encryption
  - LTE Modem

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HW/SW Design Flow: SW Programmer

- SW Programmer
- C-compiler
- AXI
- Middleware
- SW-drivers
- Hardware
- Wires
- C-synthesis
- CPU FPGA
- Hardware
- Concurrent SW
- SW
-

- Application Programming
- Video Codec
- Encryption
- LTE Modem
- Data Movement Interconnect
- Memory
- CPU
- Application
Video Acceleration

C/C++ Software Program

Main program;
Setup input;
Setup Output;
Image filter;
Edge Detect;
Motion Detect
Difference;
Draw on screen;

1 frame per 13 seconds
C/C++ Software Program

Main program; Setup input; Setup Output; Image filter; Edge Detect; Motion Detect; Difference; Draw on screen;

Software video processing functions compiled onto FPGA fabric
60 frames per second, 700x speedup
FPGA/CPU Use Models

0. Pipelined datapath
   - HDL programmed

1. Pipelined datapath with SW control
   - CPU sets register values

2. CPU + FPGA co-processing
   - FPGA part of explicit address space

3. CPU + FPGA peer processing
   - Cache Coherency
Towards Heterogeneous Multi-core

**OpenCL**

- Hardware / Software partitioning & interfacing

**C**
- Compile / Debug

**ARM Processor**
- A9

**Commercial Software Ecosystem**

**HS-SW Interfacing Domain Specific API**

**C-HLS**
- Accelerator synth

**FPGA**
- Video codec
- Encryption
- Packet Processing
- FFT
- Search

**Application-Specific**

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Opportunities for SoC Education

<table>
<thead>
<tr>
<th>Zynq</th>
<th>OS</th>
<th>Area</th>
<th>Priority</th>
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</thead>
<tbody>
<tr>
<td>Embedded</td>
<td>Linux</td>
<td>Research</td>
<td>Embedded Systems Lab</td>
</tr>
<tr>
<td></td>
<td>Standalone</td>
<td>Teaching</td>
<td>Comp. Arch., SoC</td>
</tr>
<tr>
<td></td>
<td>Other OS</td>
<td>Projects</td>
<td>DSP</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Open Source Community</td>
<td>CROME*</td>
</tr>
</tbody>
</table>

*Controls, RObotics and MEchatronics
ZED Board

- Zynq Evaluation and Development Kit
- Low cost Zynq based community board (XC7Z020)
- Partnership between Avnet, Digilent, Xilinx
- Digilent will fulfill academic market for Xilinx University Program

ZEDboard.org

Open source SW and IP
- Linux
- Eclipse based IDE
- Vivado HLS: C to FPGA
- Reference designs
Target Teaching Platform (TTP)

- Turn key solution for teaching labs on
  - Digital Logic
  - Digital Signal Processing
  - Embedded System Design
  - Principle of Microcomputers
  - Embedded Operating Systems

- Xilinx updates the kit as and when required
Targeted Teaching Platform (TTP)

Initial version of the Smart Car TTP:

ZynqBot– Mark1

Controlled wirelessly by Android cell phone app
Conclusions

- Modern FPGA is an All Programmable SoC
- Software Centric Design Flow
- Unmatched Performance/Watt
- Towards Heterogeneous Multi-Core
- Targeted Teaching Platform