FinFETs & SRAM Design

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April 19, 2013
Agenda

FinFET – the Device
SRAM Design with FinFETs
Reliability in FinFETs
Summary
How FinFETs Work

Field Effect Transistors: It is all about Gate(s) Control of the Channel

- **Planar FET**
  - Single gate channel control is limited at 20nm and below

- **FinFET**
  - "Multiple" gate surrounds a thin channel and can “fully deplete” it of carriers. This results in much better electrical characteristics.

- Better control of SCE
- Lower DIBL and lower SS
- Higher $I_{ON}/I_{OFF}$ for fixed $V_{DD}$, or lower $V_{DD}$ to achieve target $I_{ON}/I_{OFF}$

- Increasing sub-threshold leakage
- Increasing gate leakage
- Decreasing mobility
FinFET Advantages & Considerations

Clear Advantages

• Excellent short channel control leads to
  – Lower leakage (lower DIBL and lower SS)
  – Low $V_t$ variability due to low channel doping
  – Less variability caused by random dopant fluctuations
  – Lower operating voltage -> 50% dynamic power savings

Additional Considerations

• Quantized widths (and channel lengths)
• Body biasing totally ineffective
• Higher parasitics
• Potential Self-Heating issues
• Thermal aspects of ESD can be an issue
• Degradation and aging: NBTI a bit worse than planar
FinFET Device Complexity

**Side View**

- TC
- Ct
- Gate
- Fin
- Diff
- Cdiff
- Cfin
- Cg (in channel)

**Top View**

- Diff
- Gate
- Cg2
- Cf2
- Cfp

- Field Poly

- Silicide
- Gate
- Gate Oxide
- Rdiff
- R_{ext/LDD}
- Heavily-doped S/D regions
- S/D Extension Region
- Channel Region
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FinFET – the Device

SRAM Design with FinFETs

Reliability in FinFETs

Summary
FinFET SRAMs
The Good News

- Higher performance and lower leakage compared to planar
- Operates at lower Vdd than planar
- Good static noise margin (SNM) at low Vdd
  - Decent noise to signal ratio can be achieved (with a $\beta=2$ for example)
  - Good (Low) Variability
  - Read Margin and Write Margin distribution narrower than in planar

Source: Kawasaki et al, 2006 Symposium on VLSI technology Digest of Technical Papers
FinFET SRAM Challenges

- The $\beta$ ratio is a quantized number thus fine-tuning $\beta$ is not possible
  - Poses challenges for both the read and write margins
  - Requires assist circuitry for reliable operation
- Body-bias techniques are not efficient – New techniques needed
- Realizing long channel devices is litho driven (DP vs. spacer) and has limited options
  - Stack short channels in series
  - Manipulation of spacer (very limited)
  - Multi-Fin pitch

Source: Jong-Ho Lee Seoul National University Thesis
FinFET SRAM Challenges (cont.)

- Layout effects on devices critical (lonely FinFET phenomena)
- Self-heating could be a problem since fins are less efficiently cooled
  - Need to be properly modeled and accounted for
- With node scaling, channel area decreases and $\sigma V_t$ increases
  - $V_t$ mismatch issues (challenges stemming from variation of $T_{ox}$, $\varepsilon_{ox}$) and work function along the fin height
- Aging simulation is important. NBTI dominates PBTI
## SRAM Assist Schemes Survey

<table>
<thead>
<tr>
<th>TECHNIQUE</th>
<th>HELPS</th>
<th>CONCEPT</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Constant negative-level write buffer</td>
<td>Write margin</td>
<td>BL-level adjustment</td>
<td>Suitable for memory compilers</td>
</tr>
<tr>
<td>(CNL-WB)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dynamic power supply (column based)</td>
<td>Read and Write margins</td>
<td>SRAM cell voltage to be switched dynamically based on the actual read, write</td>
<td>Various techniques, some need IO VDD source. Can have dummy read issues</td>
</tr>
<tr>
<td>Negative bit-line capacitive coupling</td>
<td>Write margin</td>
<td>Improves pass-gate transistor drive compared to pull-up</td>
<td>No dummy read problems, No area/ power penalty, No external VDD needed.</td>
</tr>
<tr>
<td>Adaptive dynamic word-line underdrive</td>
<td>Read margin /Write margin</td>
<td>Forward bias/ reverse bias pull-up for higher / lower drive</td>
<td>Each done separately at the expense of the other margin</td>
</tr>
<tr>
<td>Sense AMP bit-line amplification</td>
<td>Read margin</td>
<td>Provides full BL amplification to half-selected columns. Full BL amplification</td>
<td>Significant overhead cost</td>
</tr>
<tr>
<td>Word-line lowering</td>
<td>Read margin</td>
<td>Weaken pass-gate transistor drive</td>
<td>Bad for power</td>
</tr>
<tr>
<td>BL pulsing</td>
<td>Read margin</td>
<td>Improves the discharge rate of the low-node of the cell</td>
<td>Deteriorates writability</td>
</tr>
<tr>
<td>WL pulsing</td>
<td>Read margin</td>
<td>Provides data recovery by writing back the original data prior to the disturb.</td>
<td>Deteriorates writability</td>
</tr>
<tr>
<td>Dual Supply</td>
<td>Read margin</td>
<td></td>
<td>Has power savings angle in addition to read margin improvement</td>
</tr>
<tr>
<td>RMW (Read Modify Write)</td>
<td>Read margin</td>
<td>Use pre-column sense amp. All cells are read first and re-written</td>
<td>Sense amp timing is critical</td>
</tr>
</tbody>
</table>
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- FinFET – the Device
- SRAM Design with FinFETs
- Reliability in FinFETs
- Summary
Reliability in FinFETs

- **HCl in FinFETs**: The narrower the FIN, the better the HCl immunity due to smaller half-life of the hot electrons
  - In general, HCl immunity for FinFET is better than planer

- **NBTI/PBTI (Negative / Positive Bias Temperature Instability)**: a function of the high-K gate stack not of the device.
  - In theory should be very similar to planar
  - There are indications it is worse for FinFET because of higher density of hydrogen dangling bonds at the Fin-Gate stack interface due to the <110> orientation of channel
    - More significant for FinFETs due to lower nominal Vt and nominal VDD
    - Not enough data available to establish a defined trend
Soft Error Rate – FinFETs vs. Planar

- TCAD simulation indicates that with all identical variables, SER rate in bulk FinFET-based SRAM is better than planar.

- Charge generation caused by energetic impinging particles is in the substrate. In planar, a lot of it can reach the drain.

- In FinFET, the conduction is mainly in the channel, thus most of the charge dissipates in the substrate, NOT in the drain, therefore probability of upset is much lower.
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FinFET – the Device
SRAM Design with FinFETs
Reliability Concerns

Summary
The Real Deal About FinFETs

Designers must deal with new BSIM models, new netlist parameters, quantized “W” and “L”, NF, NFIN, etc. but no major disruption in design methodology for IP users.

SRAM design techniques including body bias and various assist techniques might not work for FinFETs and require a fresh approach.

Layout migration from planar is not always feasible. High device parasitics and high device performance dependency on layout call for extreme care in layout.

HCI and SER are generally better than in planar due to thin body & elevated channel. NBTI is slightly worse.
Thank You