3D-IC is Now Real: Wide-IO is Driving 3D-IC TSV

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What the fuss is all about …

Enables 100x Improvement in Die-to-Die Bandwidth Per Watt
2-3x Capacity Advantage Over Monolithic Devices

Faster, Denser, Low-power Chips Using 3D-IC TSVs

Samsung Wide-IO Memory for Mobile Products - A Deeper Look

Xilinx brings 3D interconnect to commercialization phase in digital FPGA world
What and Why: Wide-IO and TSVs?
Customer drivers in the industry
Performance, power and area (PPA) enables end-product differentiation

Mobility is Key: Faster, Denser, Low-power Chips
Paradigm shift from 2D SOCs to 3D-ICs
Achieving the PPA goals within shorter time-to-market

**SOC: One Large Die**
- **PROS**
  - Most common today
  - Strong ecosystem
  - Cost effective for very high volume production
- **CONS**
  - Long development times
  - “Bet-the-farm” tape-outs
  - NREs and yields < 22 nm?
  - One process for Logic, Memory and Analog?
  - HW difficult to customize

**SiP: Multi-Die Wirebonded**
- **PROS**
  - Production-proven
  - Mix different processes
  - Build a system quickly
  - HW easily customized
  - Short development time
- **CONS**
  - Bonding needs I/O rings
  - Wires add RLC parasitics - limited power savings
  - Limited speed gains
  - Limited number of layers

**3D-IC TSV: Multiple Die Through Silicon Vias**
- **PROS**
  - Densest implementation
  - Low power, high speed
  - Ideal for high complexity
  - Easy to mix processes
  - 1000s of TSVs possible
  - Die- I wafer level-stacking:
    - Flexibility versus unit cost
- **CONS**
  - Ecosystem emerging
  - Volume production ramping
  - Thermal issues?
CPU to DRAM
Existing inter-die connection methods

Parallel Connection across a PCB
- Most common CPU/SoC-to-DRAM connection today
- Well understood and extensible
- Many pins required for high bandwidth
- ~60 signal pins for a 32-bit LPDDR2 interface (2012 low-mid range smartphone)
- ~120 signal pins for a 2-channel LPDDR2 interface (2012 mid-high end smartphone)
- ~300 signal pins for a 3-channel 64-bit DDR3 interface (2012 PC)

Serial Connection Across a PCB
- Fewer pins than parallel connection
- Common for PCIe and other SerDes-based standards
- Can provide data transfer over longer physical distances if needed
- Potential latency and power considerations
- Not commonly used for DRAM at present; future solution?

Pin Count, Power, Latency Concerns?
New inter-die connection method: TSV
What is Wide-IO DRAM?

Current Standard
- 4 128-bit channels
- Total 512 bits to DRAM
- 200MHz SDR
- 100Gbit/s bandwidth

Possible Future Standard
- 4 128-bit channels
- Total 512 bits to DRAM
- 1066MHz DDR (2133MT/s)
- 1Tbit/s bandwidth

Possible Future Standard
- 4 128-bit channels
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Possible Future Standard
- 2Tbit/s bandwidth
Why do you need Wide-IO DRAM?

Bandwidth Requirements of Future Mobile Devices

![Graph showing bandwidth requirements from 2012 to 2015 for tablets and cellphones]

<table>
<thead>
<tr>
<th>Solutions</th>
<th>LPDDR2 533 MHz</th>
<th>LPDDR3 800 MHz</th>
<th>WideIO 200 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Single Channel</td>
<td>Dual Channel</td>
<td>Single die + LPDDR2</td>
</tr>
<tr>
<td>Density (2014)</td>
<td>2x4 Gb</td>
<td>4x4 Gb</td>
<td>2x8 Gb</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>4.25 GBytes/s</td>
<td>8.5 GBytes/s</td>
<td>6.4 GBytes/s</td>
</tr>
<tr>
<td>Power (burst read)</td>
<td>330 mW</td>
<td>660 mW</td>
<td>430 mW</td>
</tr>
<tr>
<td>Power / Bandwidth</td>
<td>78 mW/GBytes</td>
<td>67 mW/GBytes</td>
<td>43 mW/GBytes</td>
</tr>
<tr>
<td>Cost (2014)</td>
<td>N/R</td>
<td>1</td>
<td>N/R</td>
</tr>
</tbody>
</table>

WideIO provides 2x power efficiency compared to LPDDR2/3

- The initial JEDEC proposal is providing 12.8GBytes bandwidth. Increasing DRAM frequency to 266MHz and implementing dual data rate transfers will provide eventually more than 34GBytes/s.

RTI Conference – 13th Dec 2011
A Three-Layers 3D-IC Stack including WideIO and 3D NoC
General benefits of TSVs

- **Number of connections**: Improved ~10X
- **Capacitance per connection**: Improved ~6X
- **Average Connection Length**: Improved ~200X
- **Relative power (proportional to f, c, # connections)**: Improved ~6X
Why Wide-IO is driving TSV

DRAM is the ideal candidate to drive TSV technology

• Usually manufactured on a non-logic process
• Requires high bandwidth connection between CPU and DRAM
• Uneconomic or impossible to place large capacity (Gbits) of DRAM on same die as CPU
• Low power connection between dies desirable
• Possibility of different memory configurations using the same CPU die
Implementing Wide IO and TSVs
Real chip, real example walkthrough

## Wioming test chip program

<table>
<thead>
<tr>
<th>Same SoC addressing several schemes of 3D integration</th>
<th>Proof of concept for:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wioming</td>
<td>Technology</td>
</tr>
<tr>
<td>High speed CMOS technology 70 mm²</td>
<td>Architectute</td>
</tr>
<tr>
<td>2000 TSVs</td>
<td>Design Flow</td>
</tr>
<tr>
<td>1000 bumps</td>
<td></td>
</tr>
<tr>
<td>500 balls</td>
<td></td>
</tr>
</tbody>
</table>

### Wide IO demonstrator: DRAM on Wioming
- Die to Die
- Face to Back
- TSV middle
- Cu Pillar bumps and micro-bumps
- Wide memory data bus (512-bit)
- High bandwidth (>10GBps) memory interface
- Multi-channel memory controller
- Test for 3D Memory Interconnect
- 3D floorplanning
- 3D routing (signal & power)
- 3D Test
- Verification
- Power analysis
- Thermal analysis

### 3D NoC demonstrator: Wioming on Wioming
- Die to Die
- Face to Back
- TSV middle
- Cu Pillar bumps and micro-bumps
- 3D NoC router
- 3D serial link
- Test for 3D NoC Interconnect
- TSV Fault Tolerance scheme

### 3 Layer demonstrator: DRAM on Wioming
- Combination of all above techniques

RTI Conference – 13th Dec 2011
A Three-Layers 3D-IC Stack including WideIO and 3D NoC
Wide IO SME architecture overview

- **Wide IO Memory Controller (Cadence DENALI)**
  - Compliant with DRAM specification for Wide IO from JEDEC ([http://www.jedec.org/](http://www.jedec.org/))
  - High performance, and advanced low-power features
  - First deliveries to 3D-IC Wioming ST-Ericsson/LETI project

- **Wide IO PHY Interface**
  - 200MHz, 128 bit, SDR
  - ~1200 TSVs, µbuffers and µbumps
  - Also integrates ESD protections for DRAM

- **Specific Design for Wide IO Testability Integration**
  - Boundary scan, direct access, stuck-at, memory bist, PLL test

- **Smart Memory Engine**
  - Data transfer handling between Wide IO, SRAM and ANoC
  - Integration within ANoC
  - Up to 3.2GB/s data bandwidth
## Cadence Wide-IO DRAM controller

<table>
<thead>
<tr>
<th>Challenges</th>
<th>Solutions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Merge existing and new technology</td>
<td>• Start with extensible, high performance, low-power base architecture (Supports DDR1, DDR2, DDR3, LPDDR1, LPDDR2 and now DDR4)</td>
</tr>
<tr>
<td></td>
<td>• Re-add SDR support</td>
</tr>
<tr>
<td></td>
<td>• Add new Wide IO feature support</td>
</tr>
<tr>
<td></td>
<td>• Create DFI extensions for Controller-PHY connection</td>
</tr>
<tr>
<td>New testing requirements</td>
<td>• Extend BIST engine to test for new classes of error</td>
</tr>
<tr>
<td>Verification</td>
<td>• Create memory model of Wide-IO device in Cadence VIP tools</td>
</tr>
<tr>
<td></td>
<td>• Extend existing configurable verification environment for Wide IO</td>
</tr>
</tbody>
</table>
Overview of tool and methodology

3D Technology & Design Kit

- Target technology
  - Uses ST-Microelectronics
  - Uses TSV middle (Ω) bonding
  - Is a Flip-Chip package
  - Is a Face2Back, Die-in-Package
- Back End kit
  - Virtuoso tech file and analysis
  - EDI Techno file & calculator
  - DRC & LVS « 3D » analysis

EDI 3D-IC Stack Design Implementation & Analysis

- Cadence Encounter implementation is in collaboration with STMicroelectronics on advanced systems.
- Supports a common methodology for both implementations.
- Different types of design interfaces for:
  - TSV, bump, copper pillar, backside metal layers
  - Multiple set of metal layers
- Supports multiple design implementations for:
  - Silicon interposer
  - Vertical stack
  - Mixed stack
- EDI Design methodologies are proven with a result of 300k+ layers

EDI 3D-IC Analysis Methodology

- Encounter Timing System (ETS)
- Encounter Power System (EPS)

RTI Conference – 15th Dec 2011
A Three-Layers 3D-IC Stack including WideI/O and 3D NoC

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Overview of tool and methodology

3D-ANoC TSV Floorplanning
- 3D-ANoC TSV design
  - Symmetrical 3D NoC connectivity
  - 3D NoC matrix also connected
- EDI 10.1 tool flow
  - Use automated TSV creation
  - Set die to bottom
  - Create the TSV
    - Assign TSV + A
    - Save TSV & back
  - Set die to top
    - Create front R
- Then, use semi-automated TSVs
  - Bias connections
  - Bias TSVs
  - Buffer cell placement
  - PG routing within a die
- 3D IR-Drop analysis
  - Bottom Die
    - Supplied from the Power supplies
    - 0.02 mV m
  - Top Die
    - Supplied from the Power supplies
    - 0.2 mV m

3D-IC: Power & IR drop analysis

Wioming Final

Circuit Technology
- High speed CMOS TSV middle process
- Face2Back, Die2Wafer, Flip-Chip 3D assembly

Main features
- WideI memory controllers
- 3D ANOC
- 3GPP LTE multi core CPU backbone
- ARM host CPU

Circuit numbers
- 125 Million Transistors
- 400 Macros
- 270 pads
- 1980 TSV for 3D NoC
- 1250 TSV for WideI memory
- 985 Bumps for flip chip

Circuit performances
- WideI 200MHz / 512 bits
- Units in the [350 - 400] MHz range
- Asynchronous NoC ^ 550 MHz
Cadence silicon-proven 3D-IC solution

Plan ➔ implement ➔ test ➔ verify

- Allows heterogeneous integration to offer power, performance in smallest form factor
- **Cadence is technology leader providing complete and integrated 3D-IC solution**
  - Plan ➔ implement ➔ test ➔ verify
  - 1st to market wide I/O memory controller
- **Developed in close partner-collaboration** for past 5 years with leading foundries and customers
- **Multiple 3D-IC tapeouts**
  - Multiple testchip experience: Memory over logic (28 nm), logic over analog, logic over Logic, 3-stack dies
  - Production design tapeout in mid-2010
SiP DFT /3D package test

3D DFT on Die-Level
- Insertion of 3D wrapper
- Creating Test patterns
- Verification and Simulation

Testing Die Interconnects
- ATPG for die interconnects

Testing Die in a Stack
- Modular Test approach
- ATPG-on-top test approach
Challenges in Implementation: Wide IO and TSVs
What are the challenges?

- **Manufacturing Wide-IO DRAM and assembly:**
  - Test memory wafer after production using FC bumps
  - Thin the wafer to ~50-100um thickness
  - Form TSVs and fill with metal
    - Requires elevated temperatures – extra anneal step
  - Apply backside metal and bumps
  - No opportunity to test here
    - Backside metal bump pitch too fine for most tester heads
  - Handle dies while avoiding mechanical damage
    - They are now the approximate aspect ratio of a postage stamp
  - Attach dies (and interposers, if present) together
  - Does it still work?
What are the challenges?

- Thermal Issues:
  - Where does the heat go?

- Ecosystem Issues:
  - How many parties involved in stack production?
  - How are responsibilities divided?
  - How are liabilities divided?
Cost !!!
Back of the napkin calculation

- TSV Cost? $150 - $800 wafer?
  ~800 good die/wafer?
  ~$1.20 - $1.00 per die!

Battery Cost Savings

DRAM = 25-40% battery
$5.00 bat. in cellphone
~40% Power reduction
with Wide-Io

⇒ $0.50 - $0.80 Bott

Battery is 50% of mass & thickness
Wide-Io reduces mass & thickness
of phone by ~10%?
Conclusion

- Wide-IO and TSV are real
- Cadence believes that Wide-IO DRAM is the technology that will drive adoption of TSV
- Cadence stands ready with EDA tools and IP to enable your TSV designs with real experiences and partnerships with ~8 testchips and 1 production chip already completed.