Low Power Design: Is the Problem Solved?

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Key Drivers

- Apps
- Video
- Mobility
- Cloud
- Green Tech
Low Power Design Issues Impact Profitability
Different Drivers in Different Verticals

- **Mobile/Hand-held**
  - Battery Life
  - Unit Cost (chip package)

- **Consumer/Digital Home**
  - Unit Cost (chip package)
  - Unit Cost (fans etc.)
  - Reliability

- **Network/Data Center**
  - Power Efficiency
  - Total Cost of Ownership
  - Reliability
  - Green

Low power requirements drive different design decisions:
- Product design architecture and integration decisions
- IP make versus reuse versus buy decisions
- Manufacturing process decisions
Power Closure in Design Flow

- Chip architecture and planning
- Block design and verification
- Chip integration, verification and implementation
- Sign-off
- Silicon validation

- Normalized average cost to resolve issue
- Normalized “ideal” power variability

Project Stage

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Power Closure Challenges

- No visibility during system design and early RTL
- Lots of oscillations since RTL is not power optimized
- Poor correlation between power engines from different tools
- Real software running for the first time shows activity guesses were wrong
- Different test-cases produce drastically different activity levels
- Difficult to integrate power-aware IP
- Failure to consider final package configuration leads to component failure and yield issues

Project stage:
- Chip architecture and planning
- Block design and verification
- Chip integration, verification and implementation
- Sign-off
- Silicon validation
Low Power Design 5 Years Ago

Logic is “Connected”

Power is Not “Connected”

Can be Automated

Very Difficult to Automate
Popularity of Low Power Design Techniques
(5 years ago)

Difficulty – Design Flow Impact

Low Impact

High Impact

Power Saving

High Saving

Gate-level Optimization
5%-10%
dynamic leakage

Clock Gating
~20% dynamic

MVT
~60% leakage

PSO
~95% leakage

AVS/AVFS
40%-70%
dynamic

MSV
~40%
dynamic

DVS/DVFS
30%-60%
dynamic

Adaptive Body Bias
~40% leakage

MSV:
Multi-Supply Voltage

DVFS:
Dynamic Voltage Frequency Scaling

AVFS:
Adaptive Voltage Frequency Scaling

PSO:
Power Shut-Off
A New Low Power Design Methodology

Logic is “Connected”

Power is Connected

Is Automated

IP

Libraries

Parser

Test

Synthesis

Parser

Verification

Parser

Simulation

Parser

Silicon Virtual Prototype

Parser

P+R

Is Automated

IP

Libraries

Parser

Test

Synthesis

Parser

Verification

Parser

Simulation

Parser

Silicon Virtual Prototype

Parser

P+R

Power Intent (CPF/UPF)
Popularity of Low Power Design Techniques (now)

Difficulty – Design Flow Impact

Low Impact

High Saving
- Gate-level Optimization
  5%-10%
  dynamic leakage
- Multi-Channel Length
  ~60% leakage

Low Saving
- Dual/quad Flops
  5%-25%
  dynamic leakage
- MVT
  ~60% leakage

High Impact

High Saving
- Adaptive Body Bias
  ~40% leakage
- PSO
  ~95% leakage
- AVS/AVFS
  40%-70%
  dynamic
- MSV
  30%-60%
  dynamic
- DVS/DVFS
  ~60% leakage

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What's Next?

SYSTEM REALIZATION
TLM/SW Power Modeling and Estimation

SOC REALIZATION
IP Macro Model Integration Ready IP

SILICON REALIZATION
Methodology Is the Key
A Closer Look on Low Power Verification

Complete Power Aware Verification Solution

- ESL Power Verification
  *Real-world power verification and analysis*

- Power Plan verification and Metrics
  *Automatic power intent to verification plan*

- Assertion Based Verification
  *Power assertion generation and verification*

- Closed Loop Verification
  *Complete power-aware verification methodology*

Unified Planning Metrics, and Coverage

Common Power Intent

Advanced analysis and debug environment
Early Architecture Challenge: Power Predictability
Predictable Estimation, Analysis & Optimization

How to predictably
Estimate total power?
Optimize performance/watt?

Specification/Application/Software
Chip Planning
μArchitecture Optimization
RTL Design
Synthesis
Physical Design

Real System Activity
Relative Accuracy
Real System Activity
Good Characterization
Good Characterization
Limited Vectors

Optimize @ Architecture
Optimize @ Netlist
Effect on Power
Measurement Accuracy

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1. Power Exploration (Chip Planning Solutions)
   - Design Specification
     - Power architecture
     - Power domains
     - Low-power plan
     - Standby, talk
   - Technology Libraries
   - Estimation Results
     - Power (Dynamic, Static)
     - CPF Generation
     - Power planning (Exploration)

2. TLM IP Power estimation and optimization
   - CPF Generation
   - Power planning (Exploration)

3. Dynamic Power Analysis (SoC + SW)
   - Average and peak power window
   - Built-in Power Estimation Engine
   - Optional CPF File
   - Technology Libraries
   - Palladium XP

Estimation Results
- Power (Dynamic, Static)
- CPF Generation
- Power planning (Exploration)
Conclusion

- Low power design is a “system” problem
- Methodology is key to successful low power design
  - Repeatable
  - Scalable
  - Predictable
- Future of low power design
  - System/SoC Realization
  - Silicon Realization
- Resources
  - www.powerforward.org
  - www.eda360.com