Multi-Die ASIC SiP (System in Package) Manufacturing
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- 20+ experience in Semiconductor Operations Engineering (Product Engineering, Device Physics, Reliability, Supply Chain)
- Early adopter of SiPs – shipped >5M mobile graphics processors with DDR KGD memories in 1999
Multi-Die ASIC SiP (System in Package) Overview

First ASIC-vendor to bring 2.5D to prototype silicon (Avatar) Awarded best chip-design at ARM TechCon 2013, Santa Clara

Why 2.5D has a future → Memory Wall

- Processing can see 50-75% idle times
- CPU performance is increasing 4x-8x compared to memory performance
- Power is a big issue
  - HBM uses wide-IO to reduce frequency → lower power
- IO space is limited (packaging)
  - Memory cannot become wider
- Faster data
  - USB, PCIe, SATA, all are faster now
  - Multiple interfaces vie for same DRAM
  - Larger on-chip storage is needed
  - Video/graphics is the biggest contributor

High Bandwidth Memory

- In-house design, Hard-IP
- Leveraging 2.5D die2die “channel” experience from Avatar
- e.g. on Interposer interconnect electricals, ESD, DfT, etc.
- CMOS IO driver, 1GHz/2Gbps DDR with light output loading (1 – 8mm interposer trace)
- Electrically compatible with JEDEC HBM DRAM spec
- TSMC 16FF-GL Implementation
Avatar 2.5D Solution Demonstration

Avatar logic die
- 2 Dies of an ARM Dual-Core A9 SoC on 28nm process

TSV Si Interposer
- “65-nm” 4 Front-side, 1 Back-side metal interposer

Package Assembly
- Assemble 2 die on interposer, and placement on FlipChip package substrate

High Level Goals
- Develop a complete 2.5D KGD solution
- Demonstrate reusable portfolio of verified silicon dies with a higher level of chip abstraction

SysC Modeling
- RTL design, Verification

Demo Board Hardware and software development
- P & R,GDSII

Custom die-to-die IO
- Compact, 2Gbps signalling, fit under ubump.

Reliability testing
- Thermal, Mechanical

Interposer + Cap
w/AVATAR
w/Underfill
Lid attach
# Building the Ecosystem

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**Organic Interposer:** Kyocera

**Traditional Fabs:** TSMC, GF, UMC

**Specialized Fabs:** Innotera, Tezzaron

**Memory:** High Bandwidth DRAM Stack KGD

**Specialized IP:** High speed SERDES

**Interposer optimized D2D interfaces**

**Wide-IO and HBM memory controllers, etc.**

**Detailed package reliability**

**Test tooling, e.g. Microbump wafer probing**

**ESD guidance**

**Area-IO floor planning, die P&R, integration, and verification**

**Fine-pitch probe technology for probing microbumps**

**Power, EM, thermal modeling, and ESD analysis**

**2.5D ATPG**
Additional Benefits Of 2.5D Based Design

- Yield Improvement for large SoC die
- Overall power improvement by mixing slow and fast parts
- Risk and Cost improvement due to process node mix
- Die partitioning and optimization for analog, performance, power management, etc.
- Integrating High Bandwidth Memory, flash, or other memory technologies
Challenges

Foundries
- Microbumping,
- > Interposers exceeding reticle size
- Reliability
- Cost

Interposer Foundries
- Keep Costs Low
- Optimize Number of Metal Layers
- Integrate passives

OSATs
- Low ESD environment
- Wafer level processing techniques
- Large stacked package reliability
- Costs

Semi’s IP Houses
- Standard. Committees
- New additions and requirements (D2D IOs, ESD)
- new players

KGD vendors
- Standards across suppliers on Test/DFT, delivery metrics

DFT/Test
- Probing Microbumps
- Testing out at many different levels
- High-speed testing at probe

EDA
- Integrated tools connecting core die to interposer, package substrates